REMARKS

Pending Claims

Claims 1-4, and 6 are pending. Claims 1 and 6 have been amended. No new matter has been added.

Claim Rejections Under 35 U.S.C. §103

Claims 1-4 and 6 are rejected under 35 U.S.C. §103(a) as being unpatentable over Bowen, U.S. Patent No. 6,691,301, in view of Panchul et al, U.S. Patent Publication No. 2001/0034876, and further in view of Hines, U.S. Patent Publication No. 2005/0246682. Applicants request reconsideration of the rejections in view of the foregoing amendments and for the following reasons.

Claims 1 and 6 have been amended. In particular, claims 1 and 6 are directed to the system development method and data processing system of the invention. As amended, each claim includes that restrictions which are an inhibition of dynamic instantiation and an inhibition of a start method call from the run method are imposed on the program descriptions by employing a Java program language. Support for the amendments is provided in the Specification. *See* page 15, lines 5-18 of the Specification, for example. As amended, the claims are patentable over Bowen, Panchul and Hines, whether each reference is considered individually or in combination.

In particular, Bowen is relied upon for disclosing a C-like programming language to generate logic hardware enabling the compilation of programs into synchronous hardware

thereby compiling high level algorithms directly into gate level hardware. Bowen primarily describes using Field Programmable Gate Arrays (FPGAs) which are logic circuits that can be repeatedly reconfigured in different ways. Bowen does not disclose or suggest inputting program descriptions which define a plurality of devices by employing a Java program language capable of describing parallel operations wherein restrictions which are an inhibition of dynamic instantiation and an inhibition of a start method call from the run method are imposed on the program descriptions by employing a Java program language.

Panchul is relied upon for describing the facilitation of the design of an actual hardware implementation for digital circuits using a high-level programming language, such as the Java programming language. However, Panchul does not disclose inputting program descriptions as set forth in claims 1 and 6 wherein restrictions which are an inhibition of dynamic instantiation and an inhibition of a start method call from the run method are imposed on the program descriptions by employing the Java program language. Accordingly, Panchul does not overcome the deficiencies in Bowen with respect to the invention claimed in amended claims 1 and 6.

Hines has been relied upon for disclosing programming languages and is directed to a system and method for debugging concurrent software systems. Hines is relied upon for defining clock synchronizations of devices by using barrier synchronizations, referring to paragraphs 255-261. However, the clock synchronization disclosed by Hines does not make up for the deficiency in Bowen with respect to the restrictions of inhibition of dynamic instantiation and inhibition of a start method call from the run method that are imposed on the program descriptions by employing a Java program language, according to amended claims 1

and 6. Accordingly, the rejection of claims 1-4 and 6 under 35 U.S.C. §103(a) should be withdrawn.

Conclusion

In view of the foregoing, Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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